ET 1503963210S

Figure 1

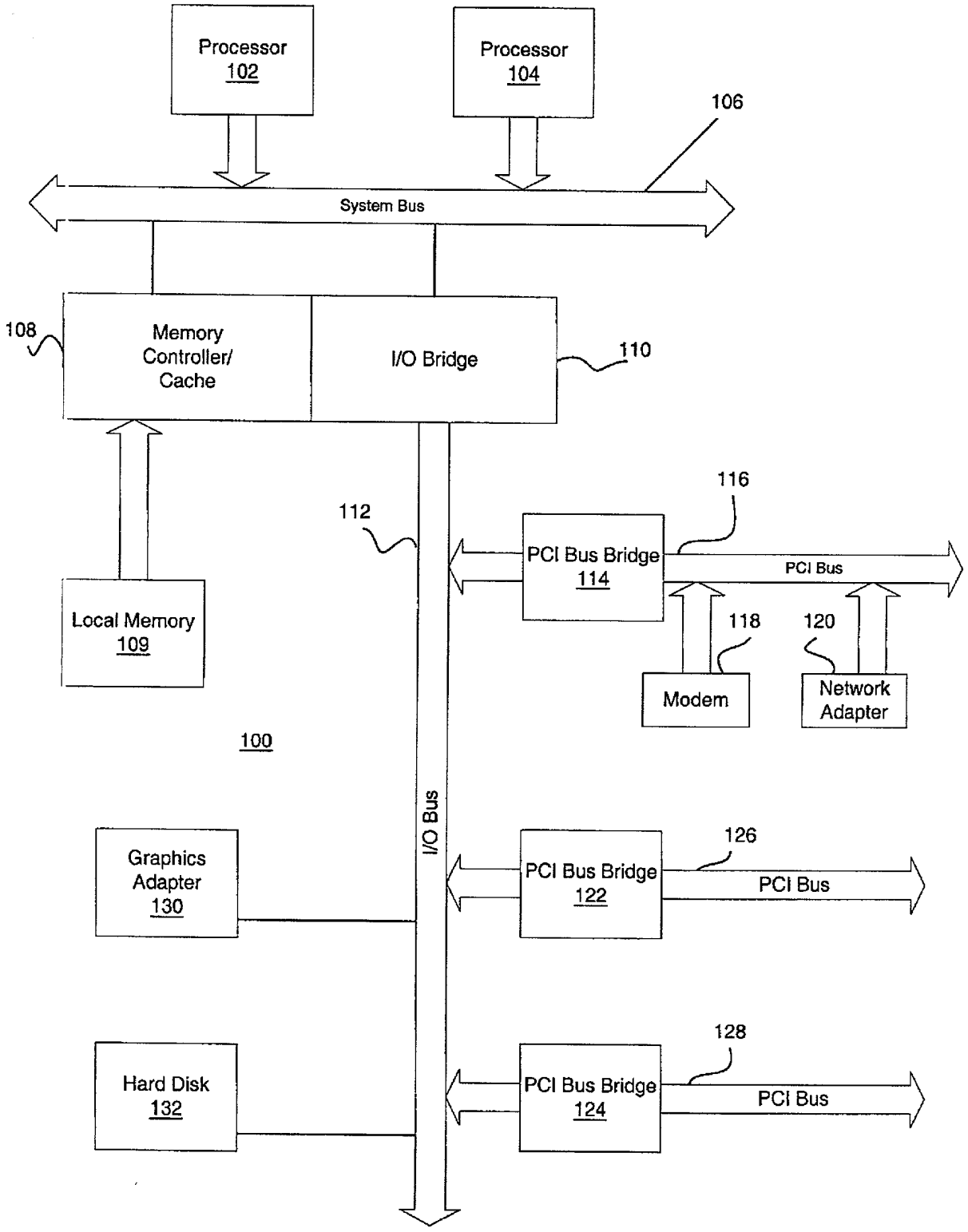
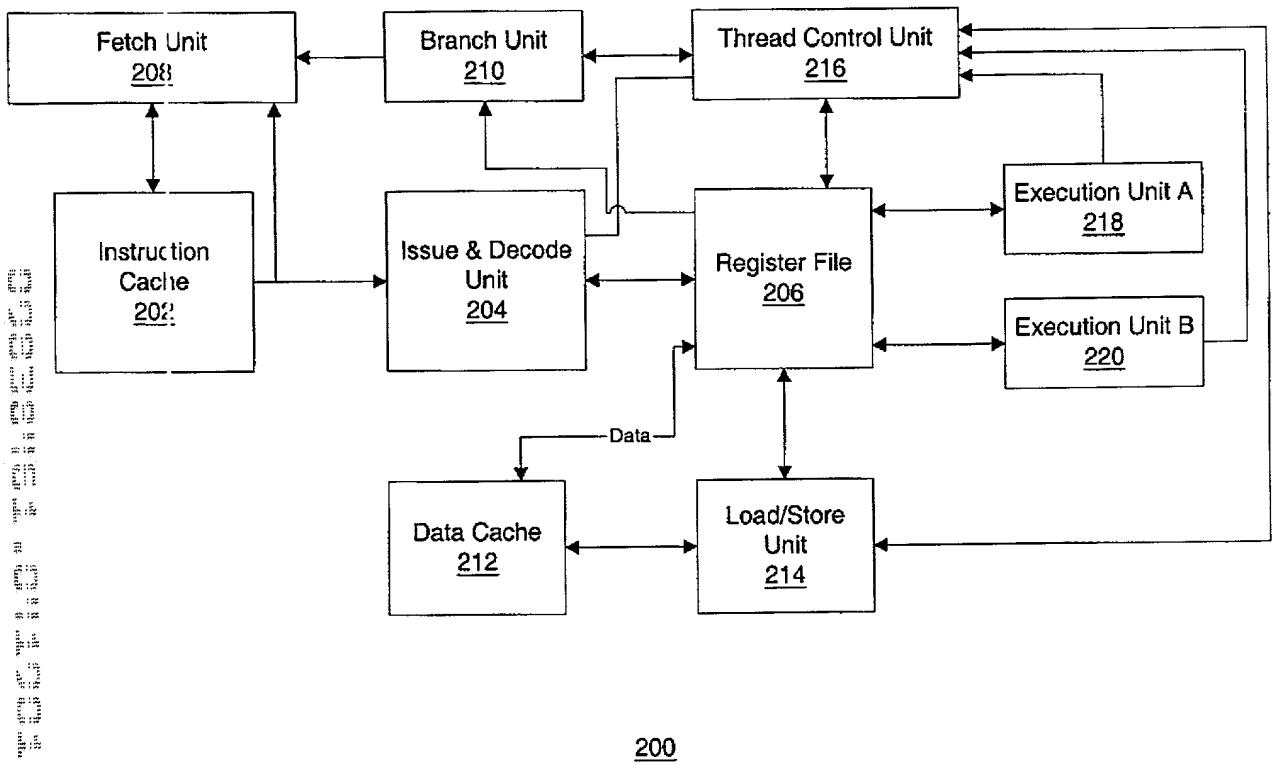
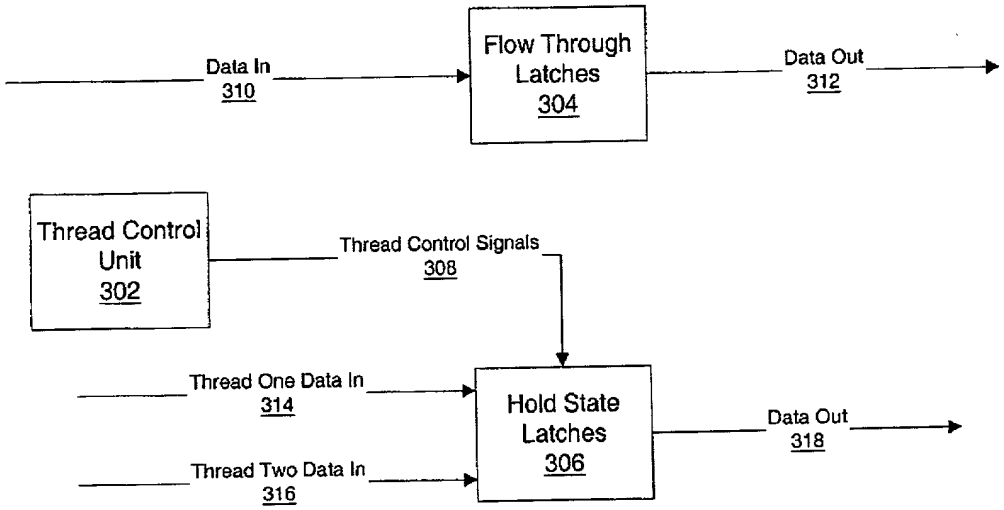


Figure 2



200
Processor

Figure 3



300
Thread Control System

Figure 4

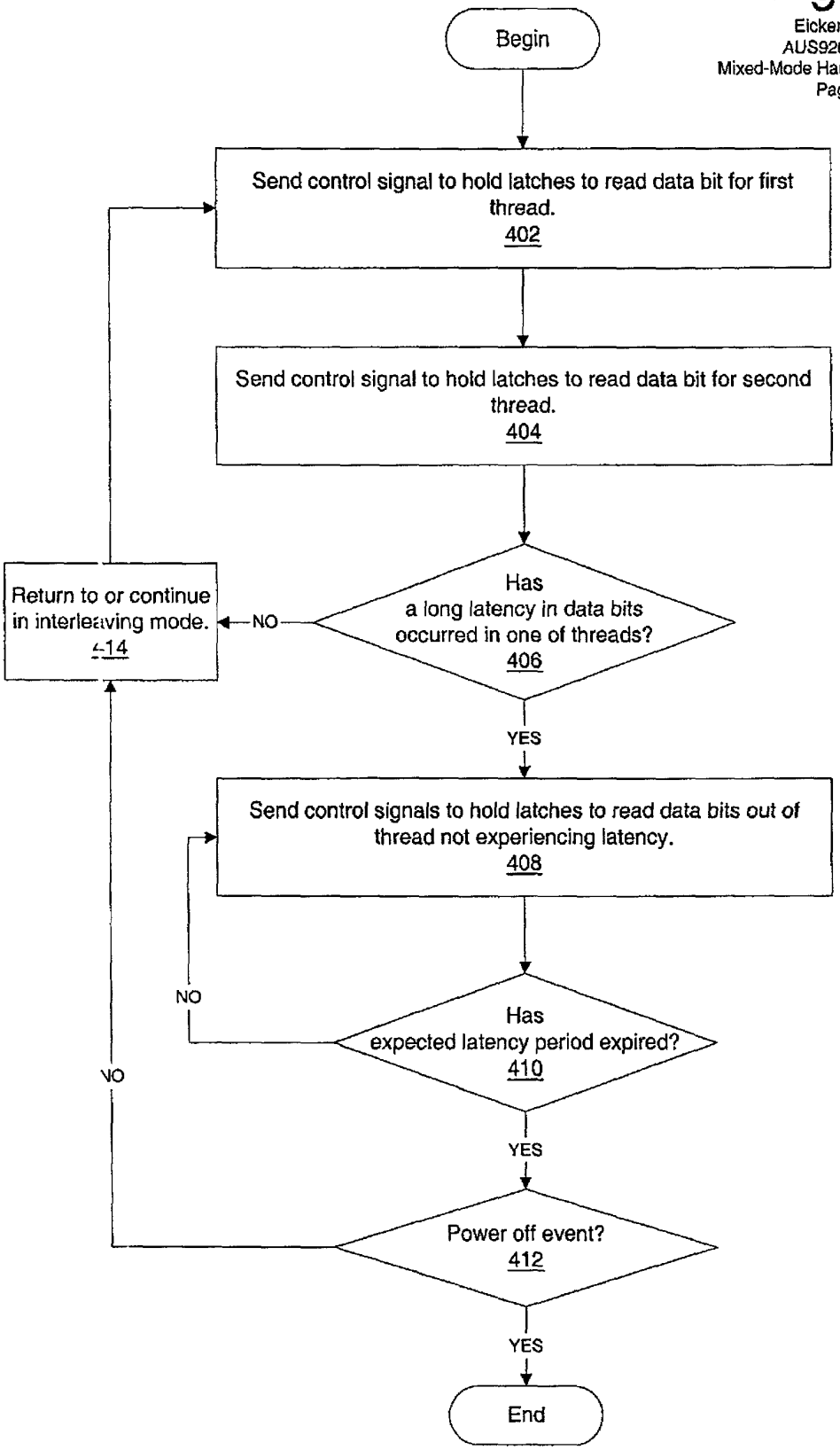
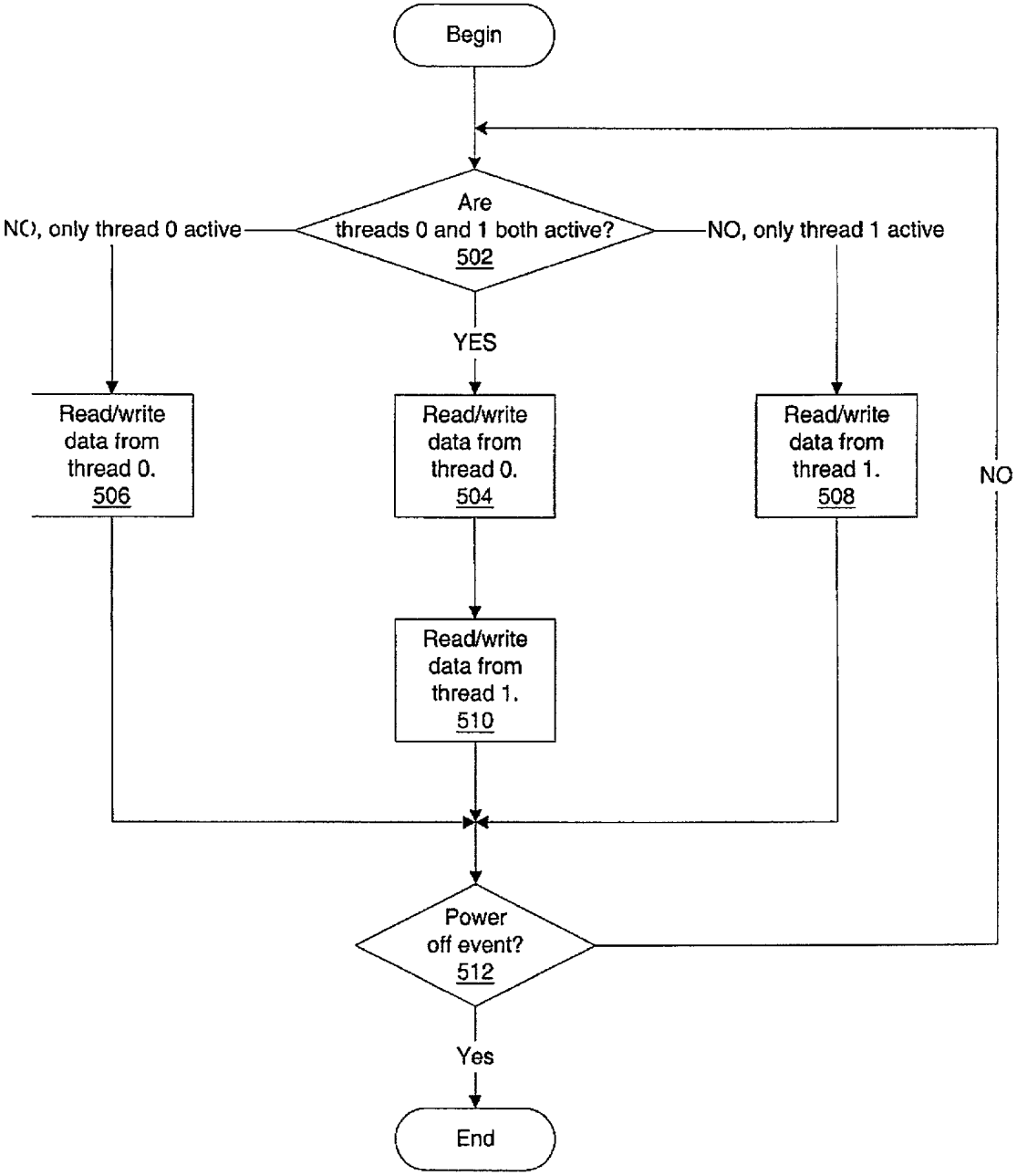

Begin
Send control signal to hold latches to read data bit for first thread.
402
Send control signal to hold latches to read data bit for second thread.
404
Has a long latency in data bits occurred in one of threads?
406
NO
Return to or continue in interleaving mode.
414
YES
Send control signals to hold latches to read data bits out of thread not experiencing latency.
408
Has expected latency period expired?
410
NO
YES
Power off event?
412
NO
YES
End

Figure 5


Begin
Are threads 0 and 1 both active? 502
NO, only thread 0 active
NO, only thread 1 active
YES
Read/write data from thread 0. 506
Read/write data from thread 0. 504
Read/write data from thread 1. 508
Read/write data from thread 1. 510
NO
Power off event? 512
Yes
End